REMARKS

Reconsideration of the application in view of the following remarks is respectfully requested.

Applicant's would like to thank the Examiner for the courtesy of the telephone interview on May 31, 2005 in which unclear points of the Official Action mailed March 2, 2005 were discussed resulting in a Supplemental Office Action being sent to Applicant's by fax that same day. In view of the fact that the original Official Action mischaracterized the Burns reference, Applicant's are replying to only the Supplemental Official Action.

The Examiner rejects claims 1-11 and 13-23 under 35 U.S.C. 103(a) as being unpatentable over Burns in view of Ryu. The Examiner states that Bums discloses a successive approximation system and method having a successive approximation value but does not explicitly disclose a successive approximation system and method that comprise a comparison system configured to amplify a difference between a test signal and a signal indicative of the successive approximation value to provide an amplified signal and to convert the amplified signal to a digital signal. The Examiner states that Ryu, in a related field, discloses an Analog/digital converter in Figure 4 that comprises a comparator which includes a differential amplifier which compares the input signals and the output of a second DAC and concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Burns' system with that of Ryu in order to suppress an increase in circuit area.

We cannot agree. The circuit of Ryu shows a differential amplifier 42 configured as a comparator 32 between the test signal and output of a second DAC. The Examiner appears to be stating that the differential amplifier comprises the summation point, the amplifier and the DAC which supplies an output to the SAR 33. Assuming, arguendo, that the differential amplifier 42 can be considered to comprise all three (3) elements, which seems unlikely, since the differential amplifier would either be configured as a comparator, as is well known to those skilled in the art, and as clearly shown in Figure 4 or as an amplifier, which would output a linear signal unless the difference signal was so great as to saturate the amplifier. Normally, one would not want a comparator to be outputting a linear signal at any time during its operation, because that would subvert the desire for a digital signal output. Even in this situation, the Ryu reference does not change the fact that both Burns and Ryu produce a single bit output to the SAR. In the present invention, once the different signal comes within the range of the ADC 422, a multi-bit digital signal is applied to the SAR 418. Which allows an increase in the resolution of the device which cannot be provided by either of the references, either singly or combined. In view of the fact that both references utilize a single bit comparison, there is no showing or suggestion of a multi-bit signal being supplied to the SAR 33 of Ryu. The fact that there is a multi-bit signal provided on line 44 from the DAC is not the same as providing a multi-bit signal on the input to the SAR 33. Accordingly, Claim 1 has been cancelled in favor of new Claim 24 and the other claims have been modified to conform, where appropriate. It should be noted that independent Claim 14 already recites "means for converting the amplified difference signal to a multi-bit digital comparison signal", which distinguishes this claim over the references cited by the Examiner and the claim has therefore not been amended.

Accordingly, Applicants believe the Application, as originally filed, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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